AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A method of ~~facilitating~~ testing ~~of~~ a pluralitv of modules in an integrated circuit, said plurality of modules comprising a first module and a second module. wherein data is transferred on a path connecting said a first module to said second module wherein said first module and said second module are to be operated together during said testing such that said second module operates using a second one of a plurality of characteristics of a first control signal when said first module is operated using a first one of said plurality of characteristics of said first control signal comprising a clock signal, said method comprising:

providing said second module with a capability of being tested in each of said plurality of characteristics of said first control signal; ~~and~~

providing a bit indicating whether a derived control signal is to be generated as a positive clock signal or a negative clock signal;

generating said derived control signal by performing XOR logical operation of said bit and said clock signal, wherein said~~providing a programmable field, which can be programmed to generate a~~ derived control signal having a desired characteristic the same as said second one of a plurality of characteristics~~, wherein said derived control signal is generated from said first control signal by programming said programmable field; and~~

~~wherein said derived control signal of said desired characteristic is~~ provid~~ed~~ing said derived control signal as a control signal to said second module; and

~~said second module is~~ teste~~d~~ing said second module with said desired characteristic of said first control signal by programming said programmable field~~,whereby said testing is facilitated even when said second module is designed for operation using a characteristic of said first control signal which is different from said characteristic of said first control signal using which said first module is designed to operate.~~

2. (Previously Presented)The method of claim 1, wherein said desired characteristic is determined to test said path at a same speed as in a functional mode of operation of said integrated circuit.

3. (Currently Amended) The method of claim 2, ~~wherein said first control signal comprises a clock signal, and~~ wherein ~~said programmable field can be set to generate~~ said derived control signal may be generated as an inverted signal of said clock signal.

4. (Cancelled).

5. (Cancelled).

6. (Original) The method of claim 2, wherein said first module comprises a core module provided by a third party not designing said integrated circuit, and said second module is designed by a designer designing said integrated circuit.

7. (Currently Amended) An integrated circuit comprising: ~~designed for testing of a first module, wherein said~~

a first module ~~is~~ to be integrated into said integrated circuit, wherein said first module is designed for operation using a first one of a

plurality of characteristics of a first control signal comprising a clock signal;~~, said integrated circuit comprising:~~

a second module provided with a capability of being tested in each of said plurality of characteristics of said first control signal, said second module being coupled to said first module by at least one path;

a test logic being programmable to generate a derived control signal having a desired characteristic, wherein said derived control signal is generated from said first control signal, and wherein said derived control signal of said desired characteristic is provided as a control signal to said second module and said second module is tested with said desired characteristic of said first control signal by programming said test logic, said test logic comprising:

a bit indicating whether said derived control signal is to be generated as a positive clock signal or a negative clock signal; and

an XOR logic gate receiving said bit and said clock signal and generating said derived control signal.

~~whereby said test logic facilitates testing of said first module and said module involving transfer of data on said at least one path between said first module and said second module even when said second module is designed for operation using a characteristic of said first control signal which is different from said characteristic of said first control signal using which said first module is designed to operate;~~

8. (Previously Presented) The integrated circuit of claim 7, wherein said desired characteristic is determined to test said path at a same speed as in a functional mode.

9. (Currently Amended) The integrated circuit of claim 8, wherein ~~said first control signal comprises a clock signal, and wherein~~ said test logic can be programmed to generate said derived control signal as an inverted signal of said clock signal.

10. (Cancelled).

11. (Cancelled).

12. (Currently Amended) ~~The integrated circuit of claim 11, wherein said test logic comprises:~~ An integrated circuit comprising:

a first module to be integrated into said integrated circuit, wherein said first module is designed for operation using a first one of a plurality of characteristics of a first control signal comprising a scan enable signal;

a second module provided with a capability of being tested in each of said plurality of characteristics of said first control signal, said second module being coupled to said first module by at least one path;

a test logic being programmable to generate a derived control signal having a desired characteristic, wherein said derived control signal is generated from said first control signal, and wherein said derived control signal of said desired characteristic is provided as a control signal to said second module and said second module is tested with said desired characteristic of said

first control signal by programming said test logic, said test logic comprising:

a bit indicating whether said derived control signal is to be generated as said rising edge triggered or said falling edge triggered scan enable signal;

a flip-flop coupled to receive said ~~original~~first control signal and being clocked on an inverted clock signal; and

a multiplexor selecting either the output of said flip-flop or said first control signal under the control of said bit.

13. (Currently Amended) The integrated circuit of claim ~~8~~12, wherein said test logic comprises a register which can be programmed.

14. (Currently Amended) The integrated circuit of claim ~~8~~12, wherein said first module comprises a core module provided by a third party not designing said integrated circuit, and said second module is designed by a designer designing said integrated circuit.